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Description

Protecting Silicon Germanium Sidewall with Silicon for Strained Silicon/Silicon Germanium MOSFETs

BACKGROUND OF INVENTION

[0001] The invention generally relates to a semiconductor device and method of manufacture and, more particularly, to a semiconductor device that includes strained silicon/silicon germanium field effect transistors with a protective silicon layer.

[0002] As silicon film thickness of Silicon On Insulator (SOI) is reduced, for high-performance CMOS fabrication, it becomes necessary to increase the thickness of source/drain regions above the SOI thickness. This results from the fact that, as the SOI film becomes thinner, a reduced amount of Si material is available from which to form silicide for source/drain contacts. Additionally, thinner source/drain regions can degrade on-current due to increased series resistance.

[0003] To maintain or reduce overall source/drain series resistance, including the silicide contact resistance, techniques have emerged to form raised source/drain (RSD) structures. For example, selective epitaxial growth of silicon has been used to grow silicon on the source/drain and the top of poly gates, leaving no silicon on gate sidewall spacers. One problem with this technique is that epitaxial growth must take place at temperatures as high as 750°C, which may cause significant transient enhanced diffusion of dopants. The unnecessary dopant redistribution in halo/extension regions degrades the performance of devices and short channel immunity. Moreover, with a very thin SOI film, it can be difficult to form epitaxial silicon without causing silicon agglomeration due to possible contamination of carbon in certain chemical vapor deposition tools.

[0004] Another technique involves SiGe selective epitaxial growth on source/drain regions. Advantageously, this technique eliminates transient enhanced diffusion of dopants which may otherwise occur at high temperatures. Unfortunately, however, Ge degrades silicide contact formation and contact resistance due to its inherent function as a diffusion barrier. To reduce such undesirable effects, the surface of

SiGe may be capped with additional epitaxial silicon, using a high temperature process, which may cause transient enhanced diffusion.

[0005] Another problem with raised silicon/silicon germanium source and drain regions involves contact formation. High quality contacts to silicon-based field effect transistors are typically achieved through a silicide process, where a metal such as cobalt or titanium is alloyed with silicon to form the contact. However, this process is generally not as effective with semiconductor materials other than silicon. For example, a cobalt silicide contact formed to a source disposed in a strained Si layer and an underlying SiGe layer may form a high-resistivity compound in the SiGe layer, thereby compromising the functionality of the contact.

[0006] The invention is directed to overcoming one or more of the problems as set forth above.

SUMMARY OF INVENTION

[0007] In a first aspect of the invention, a method of fabricating a semiconductor structure is provided. The method entails forming a raised source region on a substrate. A raised drain region is also formed on the substrate. Next, a first silicon layer is formed over the raised source region and a

second silicon layer is formed over the raised drain region.

[0008] In a second aspect of the invention, the method includes forming sacrificial spacers along the sidewalls of the first silicon layer and the second silicon layer. After forming the spacers, third and fourth silicon layers are formed on the raised source and raised drain regions, respectively.

[0009] In a third aspect of the invention, a semiconductor structure is provided. The semiconductor structure includes a substrate; a raised source region on the substrate, a raised drain region on the substrate; a first silicon layer over the raised source region and a second silicon layer over the raised drain region.

[0010] The raised source and drain regions thus include one or more silicon layers on sidewalls of the source and drain regions. The silicon prevents adverse effects of Ge during silicidation, including Ge out diffusion and silicide line breakage. The Si also increases the active area.

BRIEF DESCRIPTION OF DRAWINGS

[0011] Figure 1 shows a first side cutaway view of an exemplary semiconductor structure with a raised source and drain according to the principles of the invention;

[0012] Figure 2 shows a top view of an exemplary semiconductor

structure with a raised source and drain according to the principles of the invention;

[0013] Figure 3 shows a second side cutaway view of an exemplary semiconductor structure with a raised source and drain according to the principles of the invention;

[0014] Figure 4 shows cutaway view of an exemplary semiconductor structure with a raised source and drain and a protective silicon layer according to the principles of the invention; and

[0015] Figure 5, shows cutaway view of an exemplary semiconductor structure with a raised source and drain, a protective silicon layer and sacrificial spacers according to the principles of the invention.

DETAILED DESCRIPTION

[0016] The invention enables fabrication of raised Si/SiGe source and drain regions with epitaxially grown silicon on SiGe sidewalls. The silicon prevents adverse effects of Ge during silicidation, including Ge out diffusion and silicide line breakage. The Si also increases the active area.

[0017] Referring to Figure 1, an exemplary initial structure employed in the invention is shown. Specifically, the exemplary initial structure is comprised of an SOI substrate 105 having a patterned gate stack region 110 formed on the

surface thereof. The SOI substrate 105 may include a buried oxide layer 125 sandwiched between a top Si-containing layer 130 and a bottom Si-containing layer 140. The top Si-containing layer 130 is an area upon which devices may be formed. The Si-containing layer 130 may be comprised of various semiconducting materials that include silicon, such as Si, SiGe, SiC, SiGeC, Si/Si, or Si/SiGe.

[0018] The SOI substrate 105 employed in the present invention may be fabricated using techniques well known to those skilled in the art. For example, the SOI substrate may be formed by a conventional bonding and cutting processes, or alternatively, a conventional separation by implantation of oxygen (SIMOX) process. While the thickness of the various layers is not critical to the present invention, the top Si-containing layer 130 may have a thickness of about 5 to 250 nm.

[0019] Isolation structures, such as shallow-trench isolations (STIs) 180 and 185, are also provided in the exemplary initial structure. Techniques known in the art may be utilized to form STIs 180 and 185. A conventional technique entails patterning with a photoresist, etching the trench, chemical vapor deposition of oxide to fill the trench, and

planarizing the surface such as by chemical mechanical polishing. Subsequently, the top surface of the STI formations 180 and 185 may be etched down, as discussed more fully below.

[0020] The patterned gate stack region 110 may be formed atop the Si-containing layer using processing techniques well known in the art. For example, the patterned gate stack region 110 may be fabricated by first forming gate dielectric 125 on an exposed surface of the top Si-containing layer 130. The gate dielectric layer 125 may be formed by a conventional deposition process such as CVD or plasma-assisted CVD, or a thermal growing process such as oxidation, nitridation or oxynitridation. The gate dielectric may include any device quality dielectric material such as an oxide, nitride, oxynitride or any combination and multilayer thereof. The thickness of the gate dielectric is not critical to the present invention.

[0021] The gate stack 110 is formed on the gate dielectric 125 utilizing a conventional deposition process such as CVD, plasma-assisted CVD or plating. The gate stack 110 may include a gate material such as polysilicon, amorphous silicon or other materials suitable for MOSFET gate composition. The gate material may be formed on the surface

of gate dielectric 125 utilizing conventional deposition processes well known in the art such as, for example, CVD or plasma-assisted CVD. An optional dielectric-capping layer (not shown) may be present atop the gate material. When present, the optional dielectric-capping layer may typically be comprised of an oxide, nitride or oxynitride and formed utilizing a conventional deposition process such as, for example, CVD or plasma-assisted CVD. Alternatively, a conventional thermal growing process such as, for example, oxidation, may be used in forming an optional dielectric-capping layer.

[0022] Following formation of the gate stack 110 on the gate dielectric layer 125, the gate stack 110 and gate dielectric layer 125 are subjected to a conventional patterning process which includes lithography and etching steps. By way of example, the lithography step may entails applying a photoresist, exposing the photoresist to a pattern of radiation, and developing the pattern utilizing a conventional resist developer. Following the lithography step, a conventional etching process such as reactive-ion etching, plasma etching, ion beam etching or laser ablation may be employed in transferring the pattern to the gate stack 110 and the gate dielectric 125.

[0023] Spacers 115 and 120 are formed along gate sidewalls. For example, spacer material such as a nitride (e.g., Si_3N_4) may be deposited in a conventional manner, such as by chemical vapor deposition (CVD) using a silane source. Other techniques, which may be suitable for deposition of a nitride layer, include low-pressure CVD (LPCVD) and atmospheric pressure (CVD) (APCVD). Portions of the deposited nitride layer are subsequently etched away in a conventional manner to form the spacers 115 and 120.

[0024] After spacer formation, raised source and drain regions are formed in a conventional manner. As illustrated in Figure1, exemplary source and drain regions 160 and 175 are comprised of SiGe layers 150 and 165 capped with strained silicon layers 155 and 170. The SiGe layers 150 and 165 may be selectively epitaxially grown in a conventional manner using ultrahigh-vacuum chemical vapor deposition (UHVCVD), molecular beam epitaxy (MBE), low pressure chemical vapor deposition (LPCVD), rapid thermal chemical vapor deposition (RTCVD), and low energy plasma enhanced chemical vapor deposition (LEPECVD). Alternatively, the SiGe layers 150 and 165 may be comprised, in whole or in part, of the top silicon-containing layer 130 of the SOI substrate 105.

[0025] Silicon layers 155 and 170 may be formed on the SiGe layers 150 and 165 of the raised source and drain regions 160 and 175, respectively, using a conventional selective epitaxial silicon formation technique. For example, molecular beam epitaxy (MBE) may be used to selectively grow device quality silicon. Because Si has a smaller lattice constant (i.e., atom spacing) than Ge, when Si 155 and 170 is grown on the SiGe layer 160 and 165, the Si 155 and 170 is strained in tension. A suitable thickness for the strained Si layers 155 and 170 is below the critical thickness, which is the maximum thickness that strained Si can grow on the SiGe layers 150 and 165 without forming defects in the crystal structure (e.g., dislocations). By way of example but not limitation, the strained Si layer 155 may be approximately 5 to 100 nm thick.

[0026] Referring now to Figure 2, a top view of the exemplary initial structure is shown. Raised drain 160 and source 175 regions are provided adjacent to nitride spacer sides 115 and 120, respectively. The nitride spacer 210 surrounds the sidewalls of the gate 110. The shallow trench isolation 220, including STI sides 180 and 185, surround the active area. The cutaway view represented in Figure 1 is denoted by cutaway line A-A in Figure 2.

[0027] Referring now to Figure 3, a side view of a cutaway section represented by line B-B in Figure 2 is shown. Those skilled in the art will appreciate that the structure and process steps described below for the raised drain region apply equally as well to the raised source region.

[0028] STI oxide portions 230 and 240 are shown alongside the raised drain 160 comprised of SiGe layer 150 and strained Si layer 160. The top layer 130 of the exemplary SOI substrate may be comprised of the same material as the raised drain layer 150, namely SiGe. Thus, referring again to Figure 1, SiGe layers 150 and 165 may be comprised of the top layer of the exemplary SOI substrate. In such a case, STIs may be formed from the SOI substrate surface to the top of the buried oxide layer 135. Then, the STI oxide may be etched to reveal the raised SiGe portions of raised source and drain regions, such as SiGe layer 150 in Figure 3. This approach for raised source and drain formation may obviate the need to form layer 150 separately by epitaxial growth as described above.

[0029] Next, the raised drain 160 is protected with a silicon layer 400, as shown in Figure 4. In particular, silicon is selectively epitaxially grown on the SiGe sidewalls of the raised drain 160, forming protective silicon sidewalls 410 and

420. The selective epitaxial process also results in growth of silicon on the strained silicon layer 155, forming silicon cap 430 for the raised drain 160. The epitaxial silicon layer 400 may be formed using conventional selective epitaxial growing processes known in the art, such as molecular beam epitaxy.

[0030] In the event the width of the STI is small, a thick silicon layer 400 along the sidewalls 410 and 420 may run the risk of bridging, i.e., forming an undesired connection between features (such as source and gate or drain and gate) of the device or between features of adjacent devices. Referring now to Figure 5, to limit the thickness of the Si sidewalls 510 and 520 and avoid or reduce the risk of bridging, sacrificial oxide spacers 505 and 525 may be formed after an initial layer of silicon 500 is selectively epitaxially formed on the raised drain 160. Thus, silicon may be selectively epitaxially grown on the SiGe sidewalls of the raised drain 160, forming protective silicon sidewalls 510 and 520. The selective epitaxial process also results in growth of silicon 515 on the strained silicon layer 155. The epitaxial silicon layer 500 may be formed using conventional selective epitaxial growing processes known in the art, such as molecular beam epitaxy.

[0031] The spacers 505 and 525 may be formed along the Si coated SiGe sidewalls of the raised drain in a conventional manner, such as by oxide deposition, patterning and etching using processes known in the art. After formation of the spacers, an additional selective epitaxial growth step may be performed to complete formation of the raised drain. The oxide spacers 505 and 525 will prevent further formation of Si along the sidewalls during the additional selective epitaxial growth step. After completing the sadditional selective epitaxial growth step, the oxide spacers may be removed, such as by dry etching.

[0032] Following formation of the epitaxial silicon sidewalls 410 and 420 (or 510 and 520) and cap 430 (or 515), silicide contacts may be formed on the epitaxial silicon layer utilizing a conventional silicidation process. The presence of Ge in the SiGe underlying the silicon layer 400 (or 500) will not interfere with, degrade or otherwise adversely impact the silicidation process.

[0033] Those skilled in the art will appreciate that although Figure 1 shows only one patterned gate stack region and corresponding raised source and drain regions, the invention applies equally as well when a plurality of patterned gate stacks and corresponding raised source and drain re-

gions are formed on the SOI substrate. Thus, the invention is not limited to the embodiment wherein a single patterned gate stack region is employed.

[0034] While the invention has been described in terms of exemplary embodiments, those skilled in the art will recognize that the invention can be practiced with modifications and in the spirit and scope of the appended claims.